

650V GaN Power Transistor (FET)

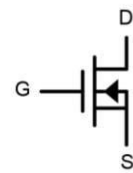
Features

- Easy to use, compatible with standard gate drivers
- Excellent $Q_G \times R_{DS(on)}$ figure of merit (FOM)
- Low Q_{RR} , no free-wheeling diode required
- Low switching loss
- RoHS compliant and Halogen-free

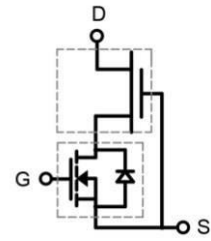
Product Summary		
V_{DSS}	650	V
$R_{DS(on), typ}$	120	m Ω
Q_G, typ	21	nC
$Q_{RR, typ}$	26	nC

Applications

- High efficiency power supplies
- Telecom and datacom
- Automotive
- Servo motors



Schematic Symbol



Cascode Device Structure

Packaging

Part Number	Package	Packaging	Base QTY
RX65T125HS2A	DFN 8 x 8	Tape and Reel	2500

Maximum ratings, at $T_C=25\text{ }^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Limit Value	Unit	
I_D	Continuous drain current @ $T_C=25\text{ }^\circ\text{C}$	18	A	
	Continuous drain current @ $T_C=100\text{ }^\circ\text{C}$	11.5	A	
I_{DM}	Pulsed drain current @ $T_C=25\text{ }^\circ\text{C}$ (pulse width: 10us)	80	A	
	Pulsed drain current @ $T_C=150\text{ }^\circ\text{C}$ (pulse width: 10us)	58	A	
V_{DSS}	Drain to source voltage ($T_J = -55\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$)	650	V	
V_{TDSS}	Transient drain to source voltage ^a	800	V	
V_{GSS}	Gate to source voltage	± 20	V	
P_D	Maximum power dissipation @ $T_C=25\text{ }^\circ\text{C}$	67.5	W	
T_C	Operating temperature	Case	-55 to 150	$^\circ\text{C}$
T_J		Junction	-55 to 150	$^\circ\text{C}$
T_S	Storage temperature	-55 to 150	$^\circ\text{C}$	
T_{CSOLD}	Soldering peak temperature	260	$^\circ\text{C}$	

Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Junction-to-case	1.85	°C/W
$R_{\theta JA}$	Junction-to-ambient ^b	50	°C/W

Notes:

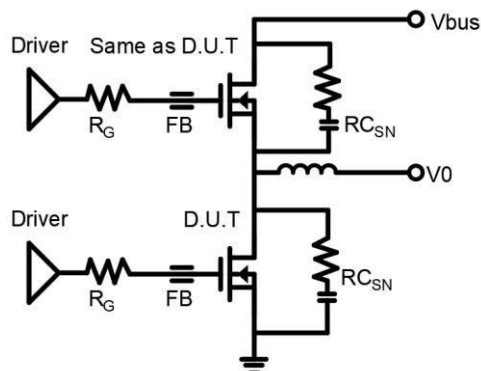
- a. Off-state spike duty cycle < 0.01, spike duration < 2us
- b. Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm² copper area and 70μm thickness)

Electrical Parameters, at $T_J=25\text{ }^\circ\text{C}$, unless otherwise specified

Symbol	Min	Typ	Max	Unit	Test Conditions
Forward Characteristics					
$V_{DSS-MAX}$	650	-	-	V	$V_{GS}=0V$
BV_{DSS}	-	1000	-	V	$V_{GS}=0V, I_{DSS}=250\mu A$
$V_{GS(th)}$	3	4	5	V	$V_{DS}=V_{GS}, I_D=500\mu A$
$R_{DS(on)}^c$	-	120	150	m Ω	$V_{GS}=8V, I_D=4A, T_J=25^\circ C$
	-	240	-		$V_{GS}=8V, I_D=4A, T_J=150^\circ C$
I_{DSS}	-	5	20	μA	$V_{DS}=700V, V_{GS}=0V, T_J=25^\circ C$
	-	50	-	μA	$V_{DS}=700V, V_{GS}=0V, T_J=150^\circ C$
I_{GSS}	-	-	150	nA	$V_{GS}=20V$
	-	-	-150	nA	$V_{GS}=-20V$
C_{ISS}	-	606	-	pF	$V_{GS}=0V, V_{DS}=650V, f=1MHz$
C_{OSS}	-	40	-	pF	
C_{RSS}	-	3	-	pF	
$C_{O(er)}$	-	57	-	pF	$V_{GS}=0V, V_{DS}=0 - 650V$
$C_{O(tr)}$	-	109	-	pF	
Q_G	-	21	-	nC	$V_{DS}=400V, V_{GS}=0 - 12V, I_D=10A$
Q_{GS}	-	6.7	-		
Q_{GD}	-	5	-		
$t_{D(on)}$	-	44	-	ns	$V_{DS}=400V, V_{GS}=0 - 12V, I_D=10A, R_G=40\Omega$
t_R	-	16	-		
$t_{D(off)}$	-	40	-		
t_F	-	12	-		
Reverse Characteristics					
V_{SD}	-	1.3	-	V	$V_{GS}=0V, I_S=5A, T_J=25^\circ C$
	-	1.9	-		$V_{GS}=0V, I_S=10A, T_J=25^\circ C$
	-	3	-		$V_{GS}=0V, I_S=10A, T_J=150^\circ C$
t_{RR}	-	16	-	ns	$I_S=10A, V_{GS}=0V, d_i/d_t=1000A/us, V_{DD}=400V$
Q_{RR}	-	26	-	nC	

Notes:

c. Dynamic on-resistance; see Figure 17 and 18 for test circuit and configurations

Circuit Implementation

Recommended Single Ended Drive Circuit

Recommended gate drive: (0 V, 12 V) with $R_{G(\text{tot})} = 34 \Omega$, where $R_{G(\text{tot})} = R_G + R_{\text{Driver}}$

Gate Ferrite Bead (FB)	Gate Resistance1 (R_G)	RC Snubber ($R_{C_{SN}}$)
MPZ1608S471ATA00	33 Ω	69 pF + 15 Ω

Notes:

- d. R_{Csn} should be placed as close as possible to the drain pin
- e. The layout and wiring of the drive circuit should be as short as possible

Typical Characteristics, at $T_c=25\text{ }^\circ\text{C}$, unless otherwise specified

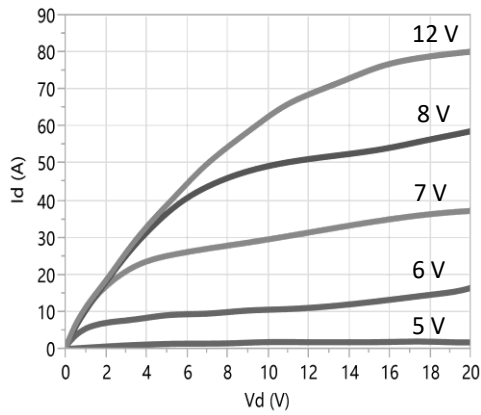


Figure 1. Typical Output Characteristics $T_j=25\text{ }^\circ\text{C}$

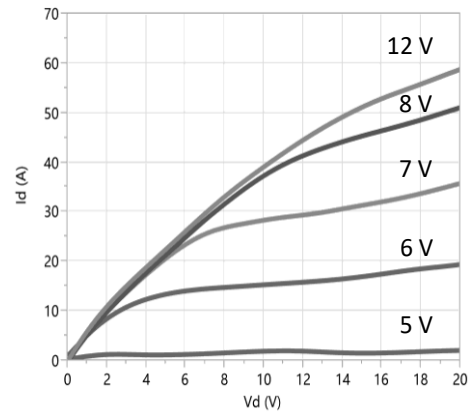


Figure 2. Typical Output Characteristics $T_j=150\text{ }^\circ\text{C}$

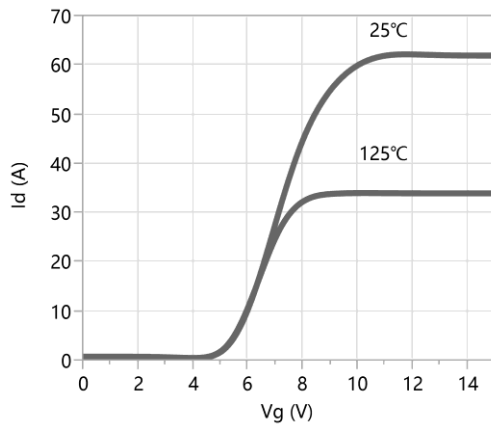


Figure 3. Typical Transfer Characteristics

$V_{DS}=10\text{V}$, Parameter: T_j

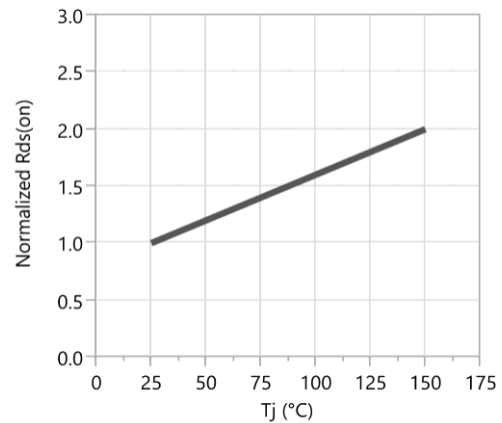


Figure 4. Normalized On-resistance

$I_D=4\text{A}$, $V_{GS}=12\text{V}$

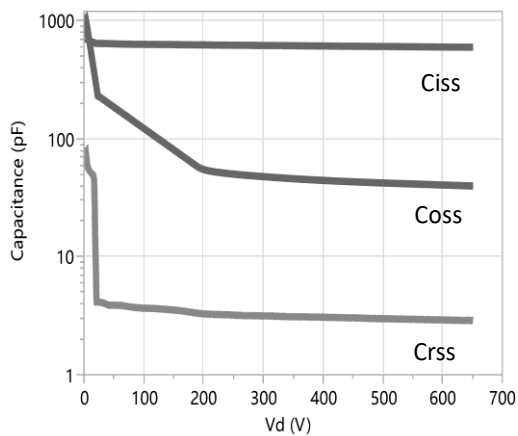


Figure 5. Typical Capacitance

$V_{GS}=0\text{V}$, $f=1\text{MHz}$

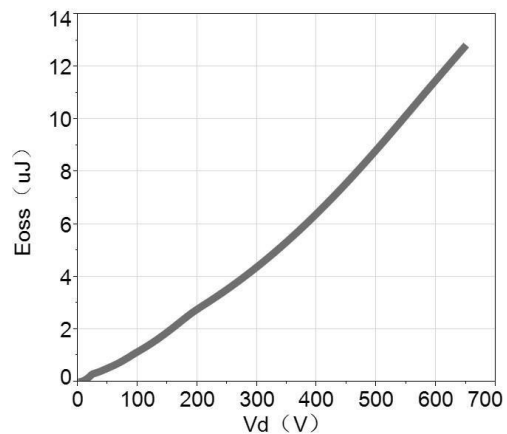


Figure 6. Typical Coss Stored Energy

Typical Characteristics, at $T_c=25\text{ }^\circ\text{C}$, unless otherwise specified

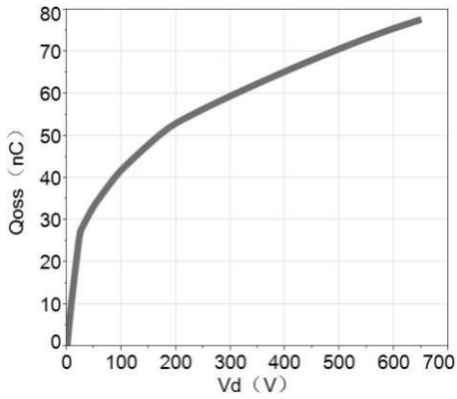


Figure 7. Typical Qoss

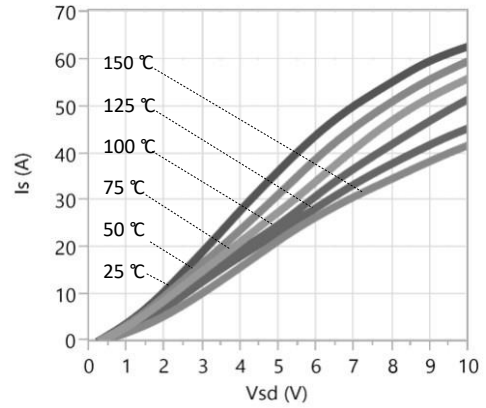


Figure 8. Forward Characteristic of Rev. Diode

$I_s=f(V_{sd})$, Parameter: T_j

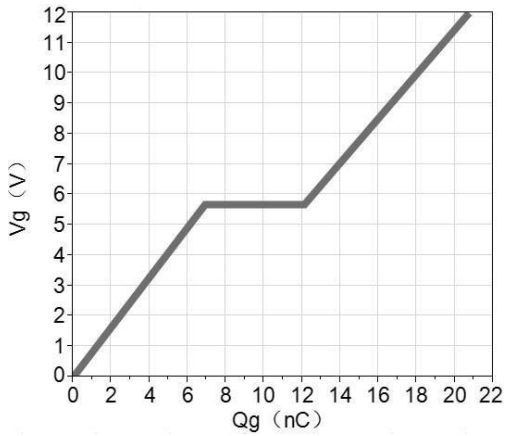


Figure 9. Typical Gate Charge

$I_{bs}=10\text{A}$, $V_{ds}=400\text{V}$

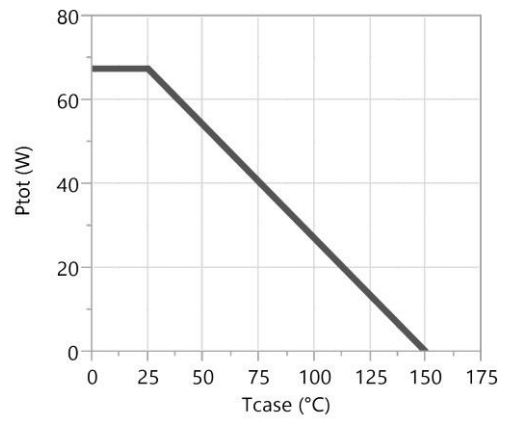


Figure 10. Power Dissipation

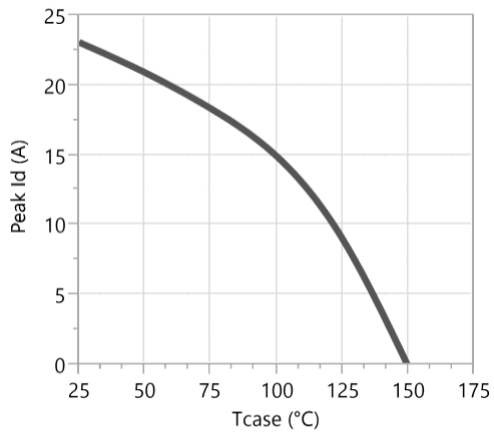


Figure 11. Current Derating

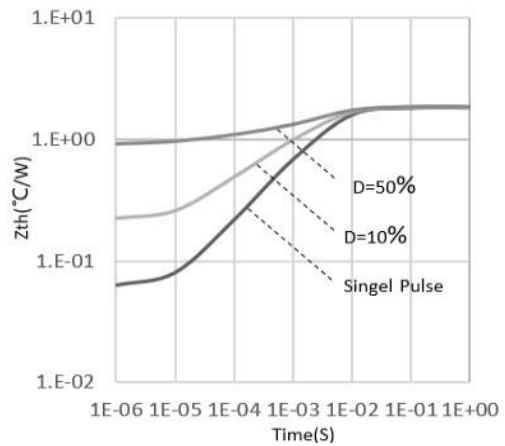


Figure 12. Transient Thermal Resistance

Typical Characteristics, at $T_c=25\text{ }^\circ\text{C}$, unless otherwise specified

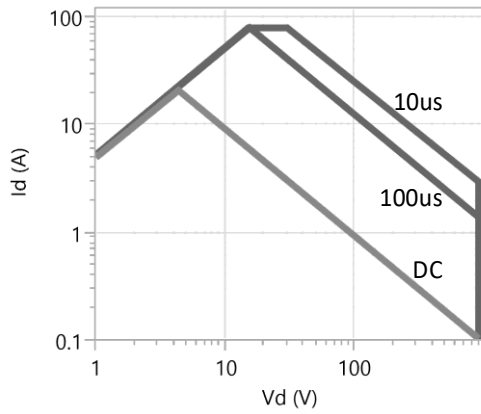


Figure 13. Safe operating Area $T_c=25\text{ }^\circ\text{C}$
(calculated based on thermal limits)

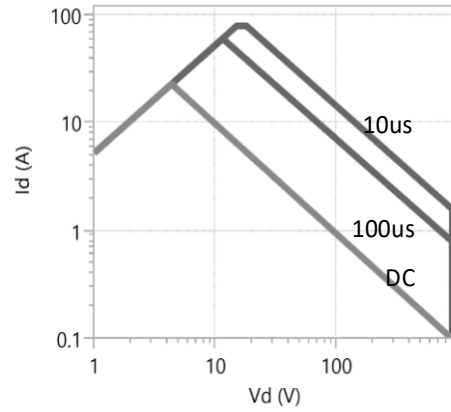


Figure 14. Safe operating Area $T_c=80\text{ }^\circ\text{C}$
(calculated based on thermal limits)

Test Circuits and Waveforms

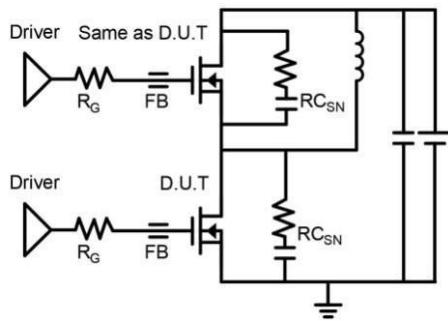


Figure 15. Switching Time Test Circuit

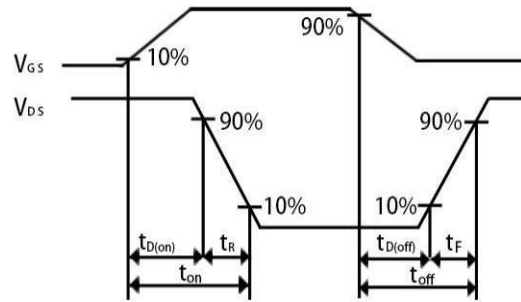


Figure 16. Switching Time Waveform

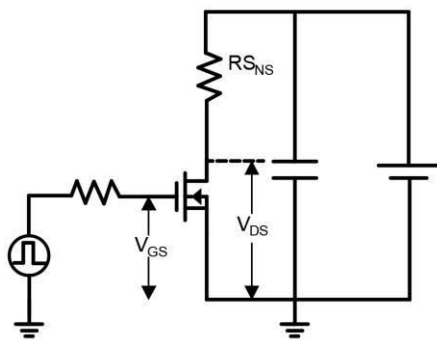


Figure 17. Dynamic $R_{DS(on)}$ Test Circuit

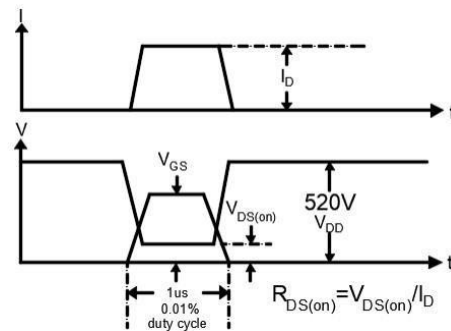


Figure 18. Dynamic $R_{DS(on)}$ Waveform

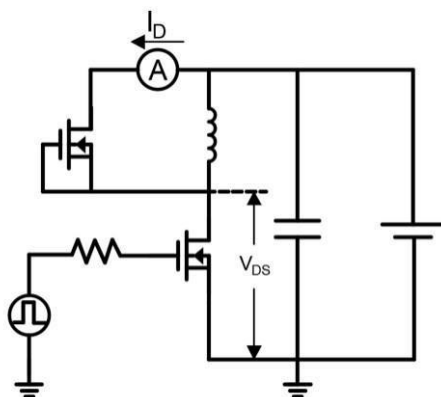


Figure 19. Diode Characteristic Test Circuit

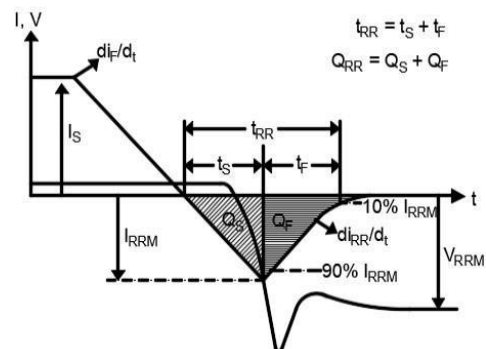


Figure 20. Diode Recovery Waveform

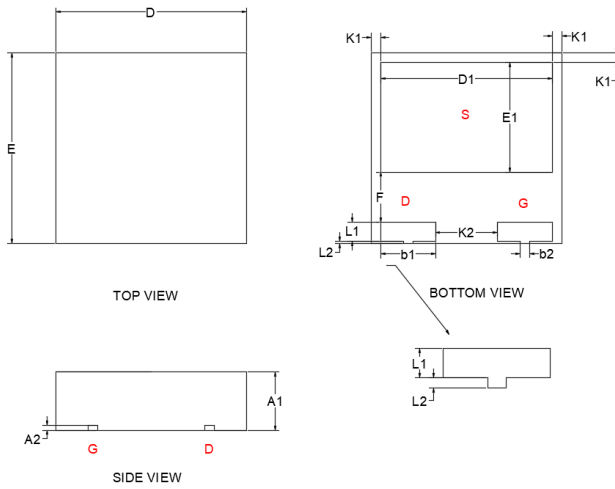
Design Considerations

Fast switching GaN device can reduce power conversion losses, and thus enable high frequency operations. Certain PCB design rules and instructions, however, need to be followed to take full advantages of fast switching GaN devices.

Before evaluating Runxin Micro’s GaN devices, please refer to the table below which provides some practical rules that should be followed during the evaluation.

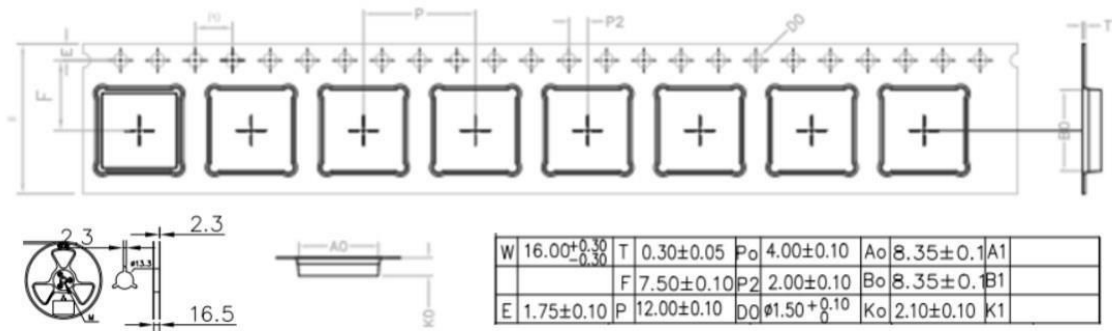
When Evaluating Runxin Micro’s GaN Devices:

DO	DO NOT
Make sure the traces are as short as possible for both drive and power loops to minimize parasitic inductance	Using Runxin Micro’s devices in GDS board layouts
Use the test tool with the shortest inductive loop, and make sure test points should be placed close enough	Use differential mode probe or probe ground clip with long wires
Minimize the lead length of TO packages when installing them to PCB	Use long traces in drive circuit, or long lead length of the devices

Package Outline

DFN 8 x 8mm (HS) Package

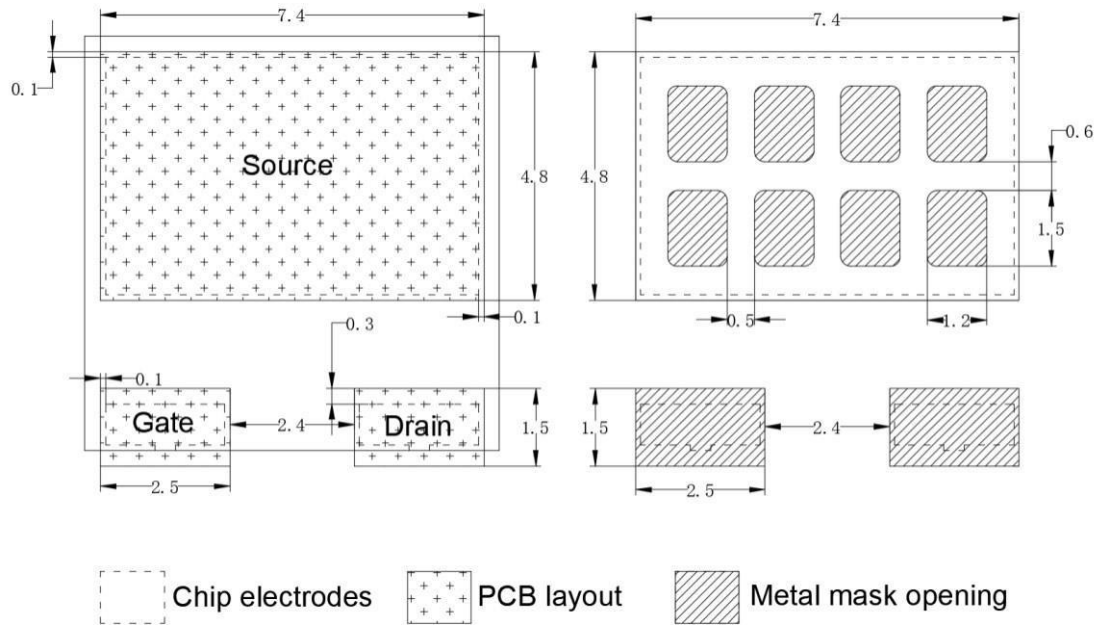
Symbol	Dimensions in Millimeters		
	MIN	NOM	MAX
A1	0.850	0.900	0.950
A2	0.195	0.203	0.211
D	7.950	8.000	8.050
E	7.950	8.000	8.050
D1	7.150	7.200	7.250
E1	4.550	4.600	4.650
K1	0.375	0.400	0.425
K2	2.575	2.600	2.625
b1	2.275	2.300	2.325
b2	0.375	0.400	0.425
L1	0.775	0.800	0.825
L2	0.075	0.100	0.125
F	2.075	2.100	2.125

Dimensions are shown in millimeters

Tape and Reel Information


Recommended PCB Layout & Metal mask opening

Dimensions are shown in millimeters


Revision History

Version	Date	Change(s)
1.0	06/24/2021	Release formal datasheet
1.1	10/27/2022	Revise $C_{O(er)}$ 、 $C_{O(tr)}$ 、 Q_G 、 Q_{GS} 、 Q_{GD}
1.2	02/01/2023	Add BV_{DSS}
1.3	03/10/2023	Revise Package Outline
1.4	05/15/2023	Revise Package Outline